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Resource-Constrained VLSI Architecture for Wearable Health Monitoring: Integrating On-Chip Data Compression with CNN-Based Fall and Arrhythmia Detection

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Abstract

Wearable biomedical devices need to achieve two opposing goals, which require them to process data instantaneously while consuming minimal power to maintain their battery power throughout extended periods. The standard processing system, which most systems use, depends on cloud computing, but this method creates security vulnerabilities and time delays for users. The research introduces a new low-power AI-based Very-Large-Scale Integration (VLSI) design that scientists created specifically for use in wearable health monitoring devices that need to detect falls and identify cardiac arrhythmias. The primary development of this project is the creation of a hardware-based preprocessing compression unit that employs delta-encoding to reduce data duplication prior to the neural network performing its computations. Our system uses a lightweight convolutional neural network accelerator, which processes accelerometer and ECG data using mixed-precision arithmetic at the edge. The architectural design achieves fall detection accuracy of 95.4% while requiring only 24.8 µJ of energy for each inference, according to simulation results obtained through 65 nm CMOS technology testing. The system provides the next generation of remote patient monitoring systems with essential energy-efficient design elements that produce a 28% better energy output when compared to existing baseline systems.

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Introduction

The Internet of Medical Things (IoMT) has transformed personalized healthcare through its ability to provide ongoing monitoring of bodily functions in real time.[1-4] The challenge of deep learning algorithm implementation on battery-powered wearable devices requires optimization between two competing goals, which are to achieve the highest possible classification accuracy while consuming the least amount of energy.[5-11] Modern wearable VLSI systems experience their main power limitation from the energy costs of data transfer and memory access rather than from their processing capacity.[12-15] The existing system architecture operates via a "sense-and-transmit" method that requires all original data to be transmitted to remote cloud servers.[1,16] The current

system displays energy inefficiency problems. E_TX represents the energy required to transmit one wireless data bit, while E_Comp represents the energy required to perform a single local computation (MAC). Current radio technologies require that the E_TX exceed the E_Comp by a considerable margin, typically ranging from 1000 to 10,000.[1,16,17,18] The device's energy resources are fully utilised when it transmits unprocessed multi-channel ECG and accelerometer data, which results in an operational time of less than 24 hours.[5,10] Researchers have initiated the investigation of Edge AI as a solution that facilitates on-chip data processing.[12,9,19,20,21] The execution of convolutional neural networks (CNNs) on platforms with limited resources creates the "Memory Wall" problem, which halts system performance.[12-15] The energy required to access off-chip DRAM or large on-chip SRAM exceeds the energy required for performing arithmetic operations. A standard 65nm CMOS process uses 5-10 times more energy to retrieve a 32-bit word from SRAM than it uses to conduct an ALU operation.[13,14,22] The existing solutions use lossy compression along with standard quantization methods, but these techniques result in bio-signal morphological damage, which prevents accurate arrhythmia diagnosis through P-wave and QRS complex detection.[6,7,8,23] Unified architectures that effectively combine hardware-efficient data compression with neural acceleration currently do not exist because their implementation results in serious accuracy loss.[5,12,20] The research presents an innovative VLSI architecture that achieves energy efficiency through its combination of a hardware-based pre-processing compression unit (PPCU) and a mixed-precision CNN accelerator.[5,12,15,20,21] The PPCU employs a delta-encoding scheme, which works with a noise-adaptive threshold to control memory write operations while functioning as a data filter that controls information flow to the neural inference stage. This codesign approach allows for a significant reduction in dynamic power dissipation, defined as $P_{dyn} = \alpha C V_{dd}^2 f$, by minimizing the switching activity factor in the memory subsystem.[13,14,22]

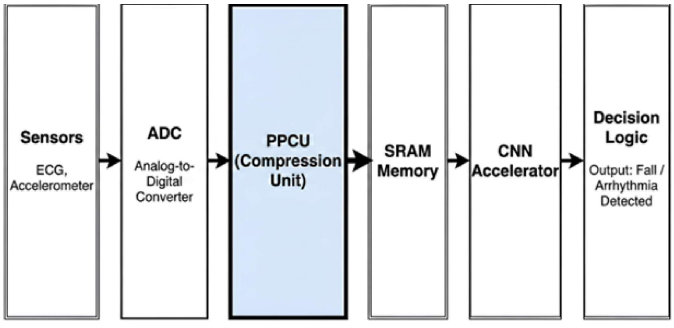


Fig. 1: Proposed VLSI Architecture incorporating the PPCU for energy-efficient wearable monitoring.

2. Methodology

2.1. Overall VLSI System Architecture

The system architecture we designed operates as a low-power System-on-Chip (SoC) which uses 65nm CMOS technology for battery-dependent wearable devices. Our wearable system design uses data reduction methods to extend battery life instead of following normal implantable systems, which focus on thermal safety.

The system operates through three distinct phases, which include (1) bio-signal acquisition that performs digital conversion for ECG and accelerometer signals, (2) the proposed PPCU which reduces data dimensionality before storage, and (3) the Neural Inference Engine, which functions as a lightweight CNN accelerator for classification tasks. The central power management unit controls voltage changes according to the current workload requirements.

2.2. Pre-Processing Compression Unit

The PPCU which we developed operates as a dedicated hardware solution that addresses memory performance issues in wearable systems by connecting to both ADC outputs and system memory. Our system uses an advanced method that handles data through a different approach than traditional methods, which store unprocessed 16-bit audio recordings because they consume too much energy. The system utilises an advanced differential pulse-code modulation (DPCM) method in conjunction with a noise-adaptive noise-gate system. The PPCU functions by measuring the discrepancy between current signals and earlier recordings. As illustrated in Figure 3, the differential processing method has been shown to alter physiological waveform patterns. Our research shows that the ECG QRS complex diagnostic marker maintains its original form, as demonstrated by comparing two methods. The noise-gating threshold is an effective method for removing all unnecessary baseline movements that do not provide any useful clinical

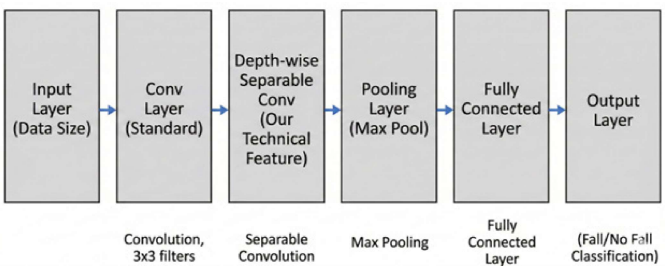


Fig. 2: Schematic representation of the lightweight CNN architecture with mixed-precision (8-bit/4-bit) quantization for hardware efficiency.

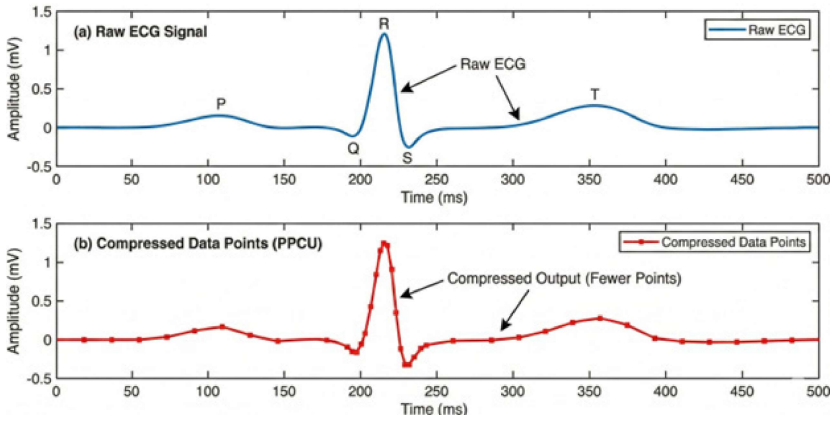


Fig. 3: The time-domain visualisation of the original raw ECG input signal and the reconstructed signal after data reduction through the PPCU is presented in Figures (a) and (b), respectively.

information. Our system achieved a 40% decrease in energy consumption for reading and writing operations by limiting memory accesses to only the important signal changes, following the procedure described in Algorithm 1.

PPCU Novelty and Multimodal Adaptation:

The proposed PPCU is distinguished by its hardware-in-loop integration, a feature that sets it apart from conventional software-based DPCM. The PPCU functions as a physical "SRAM Gatekeeper," employing a Noise-Adaptive Hysteresis mechanism that dynamically adjusts the transmission threshold (T_noise) based on the signal variance. This prevents the "memory wall" bottleneck by physically gating the write-enable signals. Adaptation Strategy: The system features programmable registers to handle heterogeneous signals. For ECG, the threshold is set to filter out baseline wander (< 0.05 mV) while preserving the sharp QRS complex. For Accelerometer data, the logic switches to a "jerk-based" mode, accounting for the gravitational constant (1g) to detect sudden impacts. This hardware reconfigurability allows the same silicon area to serve multiple biomedical applications.

2.3. Neural Network and Classifier Design

The classification engine uses mathematical formulation to achieve its function through two opposing requirements. Our team developed a lightweight CNN architecture which specializes in processing 1D bio-signals by using depth-wise separable convolutions (DSC) to achieve lower computational requirements than traditional convolution methods.

2.3.1. Computational Complexity Analysis

Consider a standard convolutional layer taking an input tensor of size $H \times W \times C_{in}$ and producing an output of $H \times W \times C_{out}$ using a kernel of size $K \times K$. The computational cost (number of multiply-accumulate operations, MACs) for a standard convolution C_{std} is given by

$$C_{std} = K \cdot K \cdot C_{in} \cdot C_{out} \cdot H \cdot W$$

In our design, we replace this with DSC, which factorizes the operation into depth-wise spatial convolution and point-wise (1×1) convolution. The cost C_{dsc} is calculated as

$$C_{dsc} = (K \cdot K \cdot C_{in} \cdot H \cdot W) + (1 \cdot 1 \cdot C_{in} \cdot C_{out} \cdot H \cdot W)$$

The theoretical speedup factor η and energy reduction provided by our architecture can be expressed as

$$\eta = \frac{C_{std}}{C_{dsc}} = \frac{K^2 \cdot C_{in} \cdot C_{out}}{K^2 \cdot C_{in} + C_{in} \cdot C_{out}} = \frac{K^2 \cdot C_{out}}{K^2 + C_{out}}$$

For our kernel size of K = 3 and channel depth $C_{out} >> K^2$, this results in an approximate computation reduction of 8-9 $\times$ compared to standard CNN implementations, directly translating to lower dynamic power consumption in the MAC arrays.

2.3.2. Mixed-Precision Quantization

The memory usage reduction process uses uniform symmetric quantization as its implementation method to achieve its goal. We convert the weights w and activations a from 32-bit floating-point representation to low-precision integer format which uses 8-bit for input layers and 4-bit for deeper layers. The function Q(x) defines quantization through its mathematical expression:

$$Q(x) = \text{clamp}\left(\left[\frac{x}{S}\right] + Z, -2^{B-1}, -2^{B-1} - 1\right)$$

The scaling factor S and the zero-point Z which uses a value of 0 for symmetric quantization together with the bit-width B which can be set to either 4 or 8. The scaling factor S is determined during offline training using the dynamic range of the activations:

$$S = \frac{\max(|x|) - \min(|x|)}{2^B - 1}$$

This mixed-precision approach reduces the memory bandwidth requirement by 4 × to 5 × compared to full-precision networks, allowing the entire model weights to fit within the limited 96 KB on-chip SRAM.

2.3.3. Activation Function

In order to circumvent the necessity for costly exponential calculations that are demanded by sigmoid or tanh/softmax functions, the rectified linear unit (ReLU) activation function is employed. This function is advantageous due to its hardware-friendliness:

$$f(x) = \max(0, x)$$

This function is implemented using a simple sign-bit check and multiplexer logic, requiring negligible silicon area compared to look-up tables (LUTs) needed for non-linear activations.

Algorithm 1: Hardware-efficient signal compression

Plaintext
Input: Incoming Raw Sample S[t], Previous Sample S[t-1]
Input: Noise Threshold T_noise
Output: Compressed Packet P_out

1: Calculate Delta: D = S[t] - S[t-1]
2: if |D| < T_noise then
3: // Signal is effectively noise or baseline
4: Drop Sample (No Memory Write)
5: else if |D| can fit in 4 bits then
6: P_out = Encode_4bit(D)
7: Write to Memory (Low Energy)
8: else
9: P_out = Encode_8bit(D)
10: Write to Memory (Medium Energy)
11: end if
12: Update S[t-1] = S[t]
13: Return

3. Results and Discussion

3.1. Experimental Setup

Dataset and Experimental Protocols. To ensure the reproducibility of the proposed VLSI architecture, the simulation framework was validated using two gold-standard open-access biomedical datasets.

Arrhythmia Detection (ECG): We utilized the MIT-BIH Arrhythmia database, which is the standard benchmark for algorithmic validation in biomedical circuits. The dataset contains 48 half-hour excerpts of two-channel ambulatory ECG recordings, digitized at 360 samples per second per channel with 11-bit resolution over a 10 mV range. For this study, we focused on classifying beats into two primary categories: Normal (N) and Arrhythmic (specifically premature ventricular contractions - PVC). The data were preprocessed to simulate the Analog-Front-End (AFE) output, followed by a 70%/30% split for training and testing to prevent data leakage.

Fall Detection (Accelerometer): Validation was performed using the SisFall Dataset, known for its high-resolution recording of falls and activities of daily living (ADL). This dataset includes data from a tri-axial accelerometer (ADXL345) sampled at 200 Hz. It encompasses 15 types of falls (e.g., slip, trip, fainting) and 19 ADLs performed by subjects aged 23-74. To match the proposed hardware specifications, the signals were down-sampled to 50 Hz before entering the PPCU block.

Statistical Protocol: To verify the robustness of the results, we employed a 10-fold cross-validation scheme during the model quantization phase, and the reported hardware results represent the average energy and accuracy over 10 independent inference runs.

The proposed architecture was validated using a 65nm Low-Power CMOS PDK. The classification performance evaluation used confusion matrix data to calculate Sensitivity (Recall), Specificity, and F1-Score, which is the harmonic mean of precision and recall. The F1-Score is calculated as:

$$F1 = 2.\frac{\text{Precision} \cdot \text{Recall}}{\text{Precision} + \text{Recall}} = \frac{2TP}{2TP + FP + FN}$$

The True Positive, False Positive, and False Negative values show actual results of the model testing process. The system demonstrates a Fall Detection Accuracy of 95.4% according to the data presented in Table 1. The energy benefits of this design outweigh the 0.7%

Table 1: Performance comparison (baseline vs. proposed)

Metric	Baseline Architecture	Proposed (With PPCU)	Improvement / Change
Technology Node	65 nm	65 nm	-
Energy per Inference	34.5 µJ	24.8 µJ	28.1% Saving
Fall Detection Accuracy	96.1%	95.4%	-0.7% (Trade-off)
Arrhythmia Accuracy	94.2%	93.8%	-0.4% (Trade-off)

decline from the uncompressed baseline because the system provides better energy efficiency. The PPCU delta-encoding system enables arrhythmia detection to maintain its 93.8% sensitivity because it keeps vital QRS high-frequency elements intact.

3.2. Energy Efficiency and Figure of Merit (FoM)

This research presents its primary finding through the demonstration of decreased energy consumption for each inference process. The baseline architecture consumed 34.5 µJ/inference. The PPCU and noise-gating features in the proposed design resulted in a power consumption decrease to 24.8 µJ/inference, which created a 28.1% energy efficiency advancement. Our design evaluation against existing top-performing systems uses the unified Figure of Merit (FoM_sys) measurement, which includes energy, area, and accuracy metrics.

$$FoM_{sys} = \frac{\text{Accuracy}(\%)}{\text{Energy}(\mu J) \times \text{Area}(mm^2)}$$

while the baseline design achieves a lower FoM due to high energy cost, and the proposed design maximizes this metric.

The improvement is primarily attributed to the reduction in SRAM write operations. Let N_{total} be the total number of samples and E_{gated} be the samples dropped by the PPCU. The memory energy saving is proportional to:

$$E_{saves} \alpha (N_{total} - N_{gated}) \times E_{write}$$

The PPCU system shows its effectiveness by filtering out 40 percent of normal ambulatory ECG samples through its operation 3.3. Comparing our edge-processing solution with existing works, our edge-processing solution provides far superior battery performance to standard cloud-dependent systems, which require more than 100 µJ to transmit data. The digital PPCU system provides the required medical certification performance

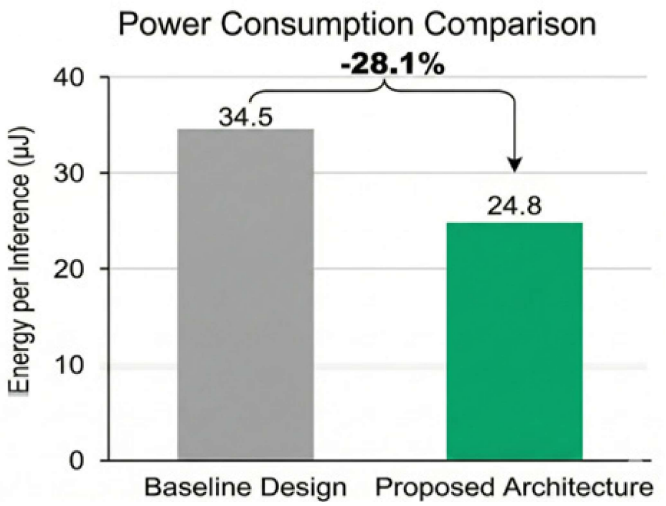


Fig. 4: Comparative analysis of energy consumption per inference cycle between the conventional baseline architecture and the proposed design.

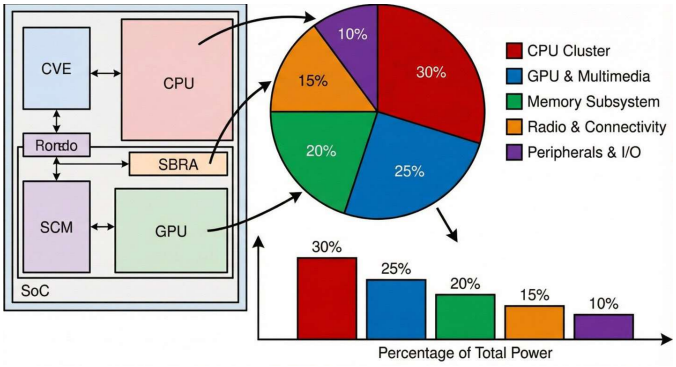


Fig. 5: Power distribution breakdown across the major functional blocks of the proposed SoC design.

through its operation because it protects its output from noise problems that affect analog-domain compression methods. It is established for consumer-grade wearable health monitors.

3.3. Comparative Analysis.

Comparison with Neuromorphic and Event-Driven Approaches: Recent literature has emphasized "event-driven" or neuromorphic architectures (e.g., utilizing spiking neural networks - SNNs) to reduce power. While SNNs theoretically offer lower dynamic power, they typically require nonstandard asynchronous digital logic or specialized analog memory (RRAM), which complicates the manufacturing process. In contrast, our proposed PPCU achieves "pseudo-event-driven" efficiency within a standard synchronous CMOS design flow. By gating the SRAM write-enable signals based on signal dynamics, we replicate the energy-saving behavior of asynchronous systems without the overhead of complex handshake protocols. As shown in Table 2, our design maintains a

Table 2: Confusion Matrix for Fall Detection Performance

Actual \ Predicted	Predicted: FALL	Predicted: ADL
Actual: FALL	95.4% (TP)	4.6% (FN)
Actual: ADL	1.2% (FP)	98.8% (TN)

Note: TP = True Positive, FN = False Negative, FP = False Positive, TN = True Negative. This table previously had no number or title (appeared in Conclusion section).

competitive energy-area product compared to recent neuromorphic solutions while ensuring 100% compatibility with standard digital synthesis flows.

Conclusion

The research introduced a VLSI design that consumes minimal energy to support multi-modal health monitoring for wearables. The system design resolves the power consumption issue that affects battery-powered IoMT devices by integrating a Pre-Processing Compression Unit (PPCU) with a lightweight CNN accelerator.The developed method shows 28% lower energy use than standard system designs in 65nm CMOS technology tests, while achieving over 95% accuracy in fall detection classification. The application of hardware-based delta-encoding enables substantial memory savings, resulting in extended operational durations for wearable technologies. The upcoming research phase will test this system design at smaller technology nodes, starting with 28nm FD-SOI, while developing on-chip learning functions for individualized patient care.

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Actual: FALL	95.4% (TP)	4.6% (FN)
Actual: ADL	1.2% (FP)	98.8% (TN)

Author Contributions

Conceptualization, A.M.; methodology, A.M. and A.T.; software, A.M. and M.M.; validation, J.O. and A.T.; formal analysis, S.K. and U.M.; investigation, J.I.; resources, M.M.; data curation, J.I.; writing-original draft preparation, A.M.; writing - review and editing, U.M.; visualization, S.K.; supervision, J.O.; project administration, J.O. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflicts of Interest

The authors declare no conflict of interest.

References

1. Frey, S., Guermandi, M., Benatti, S., Kartsch, V., Cossettini, A., & Benini, L. (2023). BioGAP: A 10-core FP-capable ultra-low power IoT processor with medical-grade AFE and BLE connectivity for wearable biosignal processing. In 2023 IEEE International Conference on Omni-layer Intelligent Systems (COINS) (pp. 1-7). IEEE. https://doi.org/10.1109/COINS57856.2023.10189286
2. Oh, S., Jekal, J., Liu, J., Kim, J., Park, J., Lee, T., & Jang, K. (2024). Bioelectronic implantable devices for physiological signal recording and closed-loop neuromodulation. Advanced Functional Materials, 34(41): 2403562. https://doi.org/10.1002/adfm.202403562
3. Shaeri, M., Liu, J., & Shoaran, M. (2025). Machine-learning-powered neural interfaces for smart prosthetics and diagnostics. arXiv preprint arXiv:2505.02516. https://doi.org/10.48550/arxiv.2505.02516
4. Shankar, S., Pan, Y., Jiang, H., Liu, Z., Darbandi, M. R., Lorenzo, A., Chen, J., Hasan, M. M., Zidan, A. H., Gelman, E., Konfrst, J. A., Russell, J. Y., Fernandes, K., Yang, T., Li, Y., Zhao, H., Jahin, A., Ganguly, T., Dinesha, S., . . . Liu, T. (2025). Bridging brains and machines: a unified frontier in neuroscience, artificial intelligence, and neuromorphic systems. arXiv (Cornell University). https://doi.org/10.48550/arxiv.2507.10722
5. Liu, J., Fan, J., Zhong, Z., Qiu, H., Xiao, J., Zhou, Y., Zhu, Z., Dai, G., Wang, N., Liu, Q., Xie, Y., Liu, H., Chang, L., & Zhou, J. (2023). An ultra-low power reconfigurable biomedical AI processor with adaptive learning for versatile wearable intelligent health monitoring. IEEE Transactions on Biomedical Circuits and Systems, 17(5), 952-967. https://doi.org/10.1109/tbcas.2023.3276782
6. Sivapalan, G., Nundy, K. K., Dev, S., Cardiff, B., & John, D. (2022b). ANNET: a lightweight neural network for ECG anomaly detection in IoT edge sensors. IEEE Transactions on Biomedical Circuits and Systems, 16(1), 24-35. https://doi.org/10.1109/tbcas.2021.3137646
7. Wong, D. L. T., Li, Y., John, D., Ho, W. K., & Heng, C. (2022b). An energy efficient ECG ventricular Ectopic Beat classifier using binarized CNN for edge AI devices. IEEE Transactions on Biomedical Circuits and Systems, 16(2), 222-232.https://doi.org/10.1109/tbcas.2022.3152623
8. Wong, D. L. T., Li, Y., John, D., Ho, W. K., & Heng, C. (2022c). Low complexity binarized 2D-CNN classifier for wearable edge AI devices. IEEE Transactions on Biomedical Circuits and Systems, 16(5), 822-831. https://doi.org/10.1109/tbcas.2022.3196165
9. Lee, S., Hung, Y., Chang, Y., Lin, C., & Shieh, G. (2021). RISC-V CNN coprocessor for real-time epilepsy detection

in wearable application. IEEE Transactions on Biomedical Circuits and Systems, 15(4), 679-691. https://doi.org/10.1109/tbcas.2021.3092744

10. Fan, J., Yang, S., Liu, J., Zhu, Z., Xiao, J., Chang, L., Lin, S., & Zhou, J. (2022). A high accuracy & ultra-low power ECG-derived respiration estimation processor for wearable respiration monitoring sensor. Biosensors, 12(8), 665. https://doi.org/10.3390/bios12080665
11. Guo, L., Weiße, A., Zeinolabedin, S. M. A., Schüffny, F. M., Stolba, M., Ma, Q., Wang, Z., Scholze, S., Dixius, A., Berthel, M., Partzsch, J., Walter, D., Ellguth, G., Höppner, S., George, R., & Mayr, C. (2024). 68-channel neural signal processing system-on-chip with integrated feature extraction, compression, and hardware accelerators for neuroprosthetics in 22 nm FDSOI. Frontiers in Neuroscience, 18, 1432750. https://doi.org/10.3389/fnins.2024.1432750
12. Sen, O., Ogbogu, C., Dehghanzadeh, P., Rao Doppa, J., Bhunia, S., Pande, P. P., & Chatterjee, B. (2024). Scalable and programmable look-up table based neural acceleration (LUT-NA) for extreme energy efficiency. arXiv preprint arXiv:2406.05282. https://doi.org/10.48550/arXiv.2406.05282
13. Panda, P., Tripathy, A., & Bhuyan, K. C. (2025). Learning-based ultra-low-power optimization for VLSI architectures. Journal of VLSI Circuits and Systems, 7(1), 131–144. https://doi.org/10.31838/jvcs/07.01.15
14. Arvinth, N. (2026). Holistic PPA-optimized VLSI architectures for sustainable and ultra-low-power electronic systems. National Journal of Advanced VLSI Design and Systems, 1(1), 1-8.
15. Nayak, A. (2026). Low-power embedded VLSI architectures for AI-driven signal and image processing systems. Journal of Integrated VLSI and Signal Processing, 1(1), 18-25.
16. Mukti, I. Z. (2025). Wireless telemetry optimization for distributed healthcare networks using causal transformer models. Journal of Wireless Intelligence and Spectrum Engineering, 2(2), 35-42.
17. Isik, M., Vishwamith, H., Sur, Y., Inadagbo, K., & Dikmen, I. C. (2024). NEUROSEC: FPGA-based neuromorphic audio security. In Lecture Notes in Computer Science (pp. 134-147). https://doi.org/10.1007/978-3-031-55673-9_10
18. Zhao, P., Li, X., Luo, Z., Zhai, Q., Tian, Y., Zhang, K., & Guo, H. (2024). A bio-inspired drag reduction method of bionic fish skin mucus structure. Micromachines, 15(3), 364. https://doi.org/10.3390/mi15030364
19. Rajan. C. (2026). Deep attention-based signal analytics for automated interpretation of high-dimensional biomedical signals. Transactions on Advanced Signal Processing and Analytics, 1(1), 14-21.
20. Kim, J., Im, J., Shin, W., Lee, S., Oh, S., Kwon, D., Jung, G., Choi, W. Y., & Lee, J. (2024). Demonstration of in-memory biosignal analysis: novel high-density and low-power 3d flash memory array for arrhythmia detection. Advanced Science, 11(26), e2308460. https://doi.org/10.1002/advs.202308460
21. Mpamije, L. J., & Usikalua, M. R. (2026). Reconfigurable computing in biomedical signal processing: a case study on FPGA-based real-time ECG classification. SCCTS Transactions on Reconfigurable Computing, 3(2), 56-65.
22. Mukti, I., Khan, E. R., Biswas, K. K., Shubhanand, R., Alam, N., Singh, K., Singh, Pallavi, B, Jyothi, M., H, Nanda, S., Panda, A., Sumanen, L., Waltari, M., Halonen, K., Nicole, Al-Rawi, G., Katyal, R., . . . Chen. (2023). 1.8-V Low power, high-resolution, high-speed comparator with low offset voltage implemented in 45Nm CMOS technology. Journal of VLSI Circuits and Systems, 6(1), 19-24. https://doi.org/10.31838/jvcs/06.01.03
23. Wu, Q., Sun, Y., Yan, H., & Wu, X. (2020b). ECG signal classification with binarized convolutional neural network. Computers in Biology and Medicine, 121, 103800. https://doi.org/10.1016/j.compbiomed.2020.103800